A COPROCESSOR CIRCUIT ARCHITECTURE, FOR INSTANCE FOR DIGITAL ENCODING APPLICATIONS

ABSTRACT OF THE INVENTION

A coprocessor circuit for processing image data in digital form, having a motion vector controller block for generating, starting from said image data, motion vector values. Such vector values include predictor data and macroblock data relating to a current macroblock of said image data to be estimated, the prediction data and macroblock data being adapted to be stored at respective memory addresses. An address generator block is provided for extracting said respective addresses from said motion vector values. A predictor fetch block for retrieving said predictor data based on respective addresses extracted by said address generator block, a current macroblock fetch and distengine block for retrieving said macroblock data based on respective addresses extracted by said address generator block and for processing said macroblock data according to a given function, all provided, as well as a decision block for collecting said retrieved data as partial results and selecting the best result therefrom.